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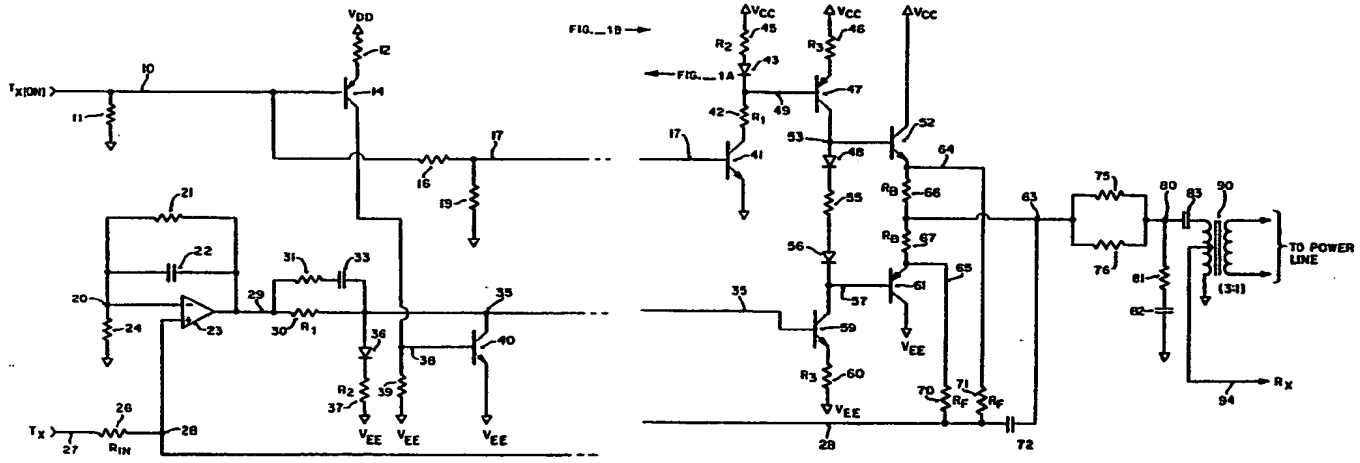

(57) Abstract

A power line communications amplifier includes a first amplifier (23) which amplifies a transmit signal consistent within a first operating potential range, a second amplifier (52, 59, 61) which provides additional amplification of the transmit signal consistent within a second operating potential range, wherein the second range is larger than the first range, and a transformer (90) which is employed to couple the amplifier transmit signal output by the second amplifier (52, 59, 61) to the power line communications system. A feedback circuit (70, 71, 72) couples the output of the second amplifier (52, 59, 61) to the input of the first amplifier (23) and functions to maintain a low output impedance while the amplifier circuit operates in a transmit mode. Control circuit (14, 40) is coupled to the second amplifier (52, 59, 61) for switching the amplifier circuit from the transmit mode to a receive mode. While in the receive mode, the amplifier circuit presents a relatively high output impedance.

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DRIVE AMPLIFIER FOR POWER LINE COMMUNICATIONS

FIELD OF THE INVENTION

The present invention relates generally to the field of amplifier circuits; more specifically, the invention relates to a class of amplifier circuits for transmitting communication signals over lines primarily used for power distribution.

BACKGROUND OF THE INVENTION

In advancing the design of communications networks, a trend is developing toward utilizing existing AC power lines as a communications medium. There is a significant advantage to the use of AC power lines for communication purposes. The installation cost for adding dedicated communication wiring and hardware to existing buildings and structures can easily exceed the cost of the system hardware itself. This provides a strong motivation to use existing power lines for communication purposes, as well as for power distribution .

In the past, there has been limited acceptance of power line communication (PLC) systems. Since power lines were never originally intended to provide a medium for communications, there are numerous problems and impairments which must be overcome in order to develop a reliable communication system utilizing existing power lines. Very often, these problems have led to inconsistent and unreliable performance in previous PLC systems.

One of the major problems which must be overcome by a PLC system is the ability to deal with the numerous noise sources and significant signal attenuation which arise in the power line environment. It is well known that most electronic and electrical products (e.g., household appliances) generate significant electrical noise which is eventually coupled back across the power lines. Attenuation of the communications signal results from the

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frequently lengthy connections and varying impedances seen at the receptacle points. Practitioners in the communications art have long recognized that the combination of signal attenuation plus high noise levels poses an especially difficult communication problem.

As will be seen, the present invention provides a drive amplifier adapted for power line communication systems. The invented amplifier circuit provides a low output impedance during transmit mode, and a high input impedance during receive mode. Special control circuitry is included to permit rapid switching between transmit and receive modes. Numerous other features desirable of a power line communications amplifier are also incorporated.

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SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved power line communications amplifier circuit which provides a low output impedance at the carrier frequency during signal transmission, and a high input impedance while in a receive mode.

It is another object of the present invention to provide an amplifier circuit for power line communications which provides a strong output signal when driving a low impedance load.

It is a further object of the present invention to provide an improved drive amplifier which draws very little power supply current while operating in a transmit mode.

It is yet another object of the present invention to provide a stable amplifier circuit for power line communications which withstands oscillation even when driving widely varying receptacle impedances.

It is still another object of the present invention to provide an amplifier circuit for power line communications exhibiting low harmonic distortion.

It is another object of the present invention to provide an amplifier circuit for power line communication systems which provides for a relatively large output voltage swing when driving a very low receptacle impedance.

It is a further object of the present invention to provide an amplifier circuit which is compatible with input and control circuitry powered from a integrated circuit operating off a standard power supply.

It is a further object of the present invention to provide an amplifier circuit for power line communications which is capable of switching between transmit and receive loads very quickly to reduce the potential for signal collisions on the line.

It is yet another object of the present invention to provide an amplifier circuit which complies with FCC regulations governing power line communications.

It is still a further object of the present invention to provide an amplifier

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circuit incorporating all of the above features at a low cost.

In accordance with one embodiment of the present invention, the amplifier circuit includes a first circuit means for amplifying a transmit signal consistent within a first operating potential range. A second circuit means provides additional amplification of the transmit signal consistent within a second operating potential range, wherein the second range is larger than the first range. A transformer is employed to couple the amplified transmit signal output by the second circuit means to the power line communications system.

The invention further includes a feedback means coupling the output of the second circuit means to an input of the first circuit means. This feedback means maintains a low output impedance while the amplifier circuit operates in a transmit mode of operation. A control means coupled to the second circuit means is used for switching the amplifier circuit from the transmit mode to a receive mode of operation. When in the receive mode, the second circuit means presents a relatively high output impedance.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A & 1B show a circuit schematic diagram of the drive amplifier of the present invention.

Figure 2 is a plot illustrating the amplifier's output impedance in receive mode as a function of frequency.

Figure 3 is a simplified circuit schematic of the present invention showing an alternative feedback configuration.

Figure 4 is a simplified circuit schematic of the present invention for illustrating an advantage of the currently preferred feedback configuration.

Figures 5A & 5B show a detailed circuit schematic of the current embodiment of the present invention including component values and part numbers.

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DETAILED DESCRIPTION

An amplifier circuit for driving communication signals onto a power line medium is described. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the invention. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well known circuits, structures, etc., have not been shown in detail in order avoid unnecessarily obscuring the present invention.

Referring to Figures 1A and 1B, there is shown a circuit schematic diagram of the amplifier circuit of the present invention. In transmit mode, the communications signal is applied to node 27. From there, it is coupled through resistor 26 to the positive input terminal of operational amplifier (op amp) 23, i.e., node 28. Phase compensation and gain for op amp 23 are provided by resistor 24, coupled between the negative input terminal of op amp 23 (i.e., node 20) and ground, and also by means of the parallel combination of resistor 21 and capacitor 22 coupled between nodes 29 and 20. Additional phase compensation is provided by the network comprising the series combination of resistors 31 and capacitor 33 coupled across nodes 29 and 35 in parallel with resistor 30.

Figures 1A and 1B also show diode 36 and resistor 37 being coupled in series between node 35 and the negative supply potential, V_{EE}. Node 35 is also coupled to the collector of NPN bipolar transistor 40. The emitter of transistor 40 is coupled directly to V_{EE} while the base of transistor 40, i.e., node 38, is coupled to V_{EE} through resistor 39. Node 35 is also coupled to the base of NPN bipolar transistor 59. Together, diode 36 and transistor 59 function as a current mirror, with resistor 30 (R_1) acting as the input resistor to the mirror. Resistor 37 (R_2) and resistor 60 (R_3), coupled from the emitter of transistor 59 to V_{EE}, establish the current ratio between the input and output of the mirror. Thus, this ratio sets the voltage gain through bipolar transistor 59 in conjunction with transistor 59's equivalent

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collector load. This aspect of the present invention will be discussed in further detail shortly.

Figures 1A & 1B also show a transmit / receive control signal, $T_{X(ON)}$, being applied to the base of PNP transistor 14 at node 10. The emitter of PNP transistor 14 is coupled to positive supply potential V_{DD} through resistor 12 while the collector of transistor 14 is coupled to the base of transistor 40 at node 38. The base of bipolar transistor 14 is also coupled to the base of transistor 41 through resistor 16. Note that nodes 10 and 17 have a path to ground provided for them through respective resistors 11 and 19.

NPN bipolar transistor 41 is shown having its emitter grounded and its collector coupled to the base of PNP transistor 47 at node 49 through resistor 42. The series combination of resistor 45 and diode 43 connect the positive supply potential V_{CC} to the base of transistor 47 at node 49. The emitter of transistor 47 is coupled to V_{CC} through resistor 46. It should be apparent that the combination of diode 43, transistor 47 and resistors 42, 45 and 46 form a current mirror in the same way described above. As before, the ratio of resistors 45 and 46 establishes the current ratio between the input and output of the mirror.

Notice that the values of resistors 42 (R1), 45 (R2) and 46 (R3) are the same as those of resistors 30, 37 and 60, respectively. This means that the upper current mirror, supplying the drive current for NPN transistor 52, matches the lower current mirror, which supplies base drive current for PNP transistor 61. Because both current mirrors drive their respective halves of the output stage (comprising transistors 52 and 61) the circuit is balanced with respect to op amp 23 (providing of course that transistor 41 is on, i.e., $T_{X(ON)}$ is high).

Continuing with the description of the circuit, NPN transistor 52 is connected to the collector of transistor 47 at node 53. The base of transistor 52 is also coupled to the base of PNP transistor 61 through the series connection of diode 48, resistor 55 and diode 56. The emitters of

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transistors 52 and 61 are coupled through biasing resistors 66 and 67.

It is appreciated that transistors 52 and 61 are arranged in a push-pull configuration wherein the collectors of transistors 52 and 61 are coupled to supply potentials V_{CC} and V_{EE}, respectively. Since the current mirrors driving transistors 52 and 61 are balanced, this means that the push-pull output stage is itself balanced. That is, if op amp 23 outputs zero volts at node 29, then the output at node 63 will also be zero. A positive output from op amp 23 causes more drive current to be drawn from transistor 61 relative to transistor 52 so that node 63 becomes more negative. Similarly, if op amp 23 produces a negative output, transistor 52 will receive more base current compared to transistor 61, and node 63 will become more positive.

Feedback is provided for in the circuit of Figures 1A & 1B by means of resistors 70 and 71 and also capacitor 72. Resistor 71 is connected between the emitter of transistor 52 (node 64) and the positive input terminal of operational amplifier 23. Likewise, the emitter of PNP transistor 61 is also coupled to node 28 through resistor 70. Resistor 70 is coupled between nodes 65 and node 28. Capacitor 72 is shown being connected across nodes 63 and 28.

Recognize that transistor 59 provides voltage gain for the amplifier circuit at the same time that the push-pull output stage provides current gain. Both of these stages operate to drive a communications signal across a pair of resistors 75 and 76. Resistors 75 and 76 are coupled in parallel across nodes 63 and 80. Node 80, in turn, is coupled to ground through resistor 81 and capacitor 82, and to one winding of transformer 90 through AC coupling capacitor 83. Transformer 90 provides an interface between the driving amplifier circuit of the present invention and the power lines. Currently, transformer 90 comprises a transformer having a 3:1 turns ratio.

Practitioners familiar with PLC systems will realize that in certain situations, signal attenuation can be minimized by the use of a power line coupling network. When used in conjunction with the present invention,

such a coupling network would be connected on the line side of transformer 90. A coupling circuit for use in PLC systems is described in a co-pending application entitled, "Power Line Coupling Network", Serial No. _____ ; filed _____ , which application is assigned to the assignee of the present invention.

Having thus far described the various connections and devices utilized in the amplifier circuit of Figures 1A and 1B, a discussion of various operating principles and advantages of the present invention may now be presented.

One of the important features of the present invention is its ability to transmit a communications signal at the carrier frequency with a low output impedance (e.g., less than 10 ohms). In transmit mode, a very low output impedance is desired in order to overcome the very low impedance of electrical appliances connected to the line. For the current embodiment, transmissions take place at a carrier frequencies of 118 kilohertz and 134 kilohertz.

Not only must the driving amplifier provide a low impedance in transmit mode, but it also must provide a relatively high output impedance (greater than 500 ohms) at the carrier frequency while in a receive mode. One can imagine that if a great many amplifiers were connected to a common power line, and if each had a low output impedance in its receive mode, then the collective load impedance as seen by a transmitting source would be so low as to make it prohibitively difficult to transmit a signal onto the line. As discussed further below, the present invention achieves a relatively high output impedance in receive mode and a relatively low impedance in transmit mode. Moreover, the invention is capable of rapidly switching between the transmit and receive mode with corresponding switching of input impedance levels as seen from the power line. This latter ability is critical for minimizing signal collisions on the power lines.

During normal transmitting operations, the transmit signal is applied to the positive input terminal of operational amplifier 23 via node 27. The

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amplified transmit signal appears at nodes 29 and 35 having a peak-to-peak amplitude which basically extends from the positive to negative operating potentials. This signal is then coupled to node 35 at the base of NPN bipolar transistor 59. As discussed above, transistor 59 provides voltage gain for the signal as it is delivered to the output stage.

It is significant to note that the portion of the circuit represented in Figure 1B is powered by the supply potential V_{CC}, which in the currently preferred embodiment represents a relatively high positive potential of approximately +12 volts (V_{EE} = -12V). At the same time, the portion of the circuit represented in Figure 1A is powered by V_{DD} (e.g., 5 V). Thus, the relatively small amplitude signal output by amplifier 23 eventually is gained up to a larger amplitude signal by transistor 59. This larger signal is output onto the line by the push-pull output stage comprising transistors 52 and 61. This stage provides current gain for the output amplifier signal.

Whenever a communication signal is being transmitted onto the power line medium, the transmit control signal, $T_{X(ON)}$, is raised to a high logic level (e.g., 5 volts). A high potential at node 10 turns off transistor 14. At the same time, transistor 40 is also turned off -- its base being grounded through resistor 39. Turning off transistor 40 allows the voltage at node 35 to swing freely.

With $T_{X(ON)}$ raised to 5 volts, a high potential also appears at node 17, thereby providing drive current to the base of transistor 41. Because transistor 41 is on, current flows through resistors 45, 42 and diode 43. The resulting voltage drop at node 49 turns on PNP transistor 47 which, in turn, provides a source of base current to activate the push-pull output stage comprising transistors 52 and 61 as explained earlier.

Diodes 48 and 56, together with resistor 55, insure that an adequate voltage separation is maintained between nodes 53 and 57 so that transistors 52 and 61 operate in the linear or active region. During

transmission the output impedance appearing at node 63 is kept to a minimum by means of the negative feedback provided to operational amplifier 23 through resistors 66, 67 and 71, 70. Basically, the output impedance of the amplifier is reduced inversely proportional to the loop gain of the amplifier and the feedback circuit.

The circuit is switched to a receive mode by taking the transmit control signal to a low logic level (e.g., ground). Grounding node 10 activates PNP transistor 14. With PNP transistor 14 on, drive current is supplied to the base of NPN transistor 40. This turns transistor 40 on, thereby pulling node 35 down to negative supply potential V_{EE}, which turns off NPN transistor 59.

Referring now to the upper half of the amplifier circuit, a ground potential on node 10 also grounds node 17. This turns off transistor 41 which causes a high potential at node 49 turning off transistor 47. With transistors 47 and 59 both off, the push-pull output stage comprising transistors 52 and 61 are disabled, i.e., the transistors have no drive current. Disabling the push-pull output stage results in a high output impedance at node 64 and 65. Hence, grounding the control signal $T_{X(ON)}$ causes the amplifying portion of the circuit of Figure 1A and 1B to switch to a high impedance state. In this state the received communication signal is simply tapped off of the amplifier side of transformer 90 (node 94).

As previously discussed, the invented amplifier is capable of switching between transmit and receive modes of operation very quickly -- with typical speeds on the order of 10 microseconds. The ability to rapidly switch between one mode of operation and the other is crucial to the avoidance of collisions between signals on the power line medium. As the switching delay gets larger, the probability of incurring collisions increases dramatically. To achieve fast switching, several important circuit features have been incorporated in the present invention.

First of all, providing an input node which can be driven digitally by standard logic devices is important in providing a control element for

switching operations. All of the components shown in Figure 1A can be easily integrated into a single semiconductor circuit using conventional bipolar complimentary metal-oxide-semiconductor (BiCMOS) process technology. Alternatively, a conventional CMOS process can be used with appropriate substitution of transistors 14, 40 and diode 36. This means that the switching circuitry of the amplifier is easily interfaced to the switching control signal $T_{X(ON)}$. Moreover, when the circuit portion illustrated in Figure 1A is fabricated as an integrated circuit, all the control and input circuitry can be powered off of a common 5 volt power supply.

It should be understood that when the circuit portion of Figure 1A is fabricated as an integrated circuit, that there will be a corresponding shift in supply voltages. For example, one possibility is $V_{DD} = 5$ volts, $V_{EE} = OV$ and $V_{CC} = +24V$. Furthermore, it is appreciated that some resistor values may need to be adjusted (e.g., resistors 42, 45 and 46) to accommodate this shift in supply voltage.

Secondly, the values of resistors 11, 12 and 39 are chosen to insure that transistor 14 always operates in a mode where it is either functions as a current source or it is completely turned off. Transistor 14 is deliberately kept out of saturation so that node 38 can be switched quickly from a high to a low voltage level. Furthermore, the presence of resistor 11 allows rapid discharge of the base voltage of transistor 14 during a high to low transition of node 10. Correspondingly, the presence of resistor 39 helps in the rapid discharge of the voltage at node 38 to turn off transistor 40. Resistor 19 performs the same function to discharge node 17, coupled to the base of transistor 41, when the control signal $T_{X(ON)}$ transitions from a high to a low level. Altogether, the DC biasing keeping transistor 14 out of saturation and the inclusion of resistors 11, 19 and 39 facilitate rapid switching between modes.

One of the difficulties in designing an amplifier circuit for driving power line communications is the fact that government regulations limit the amount of power that may be broadcast at certain frequencies. According to

the present invention, the power delivered to the line is kept relatively high without harmonic levels which would exceed government regulation limits. This is accomplished by means of transistor 59 and push-pull transistors 52 and 61, and the configuration wherein the relatively small output of op amp 23 is stepped up to a larger signal. As explained previously, transistor 59 provides voltage gain while current gain is provided by the push-pull combination. At present, the output stage of the invented amplifier circuit is capable of delivering about 40 milliamps with a communications signal of 18 volts peak-to-peak at node 63.

Recognize that the operating supply potential of the output driver stage illustrated in Figure 1B is currently maintained at approximately 24 volts (e.g., ± 12V). Because of the relatively large currents and voltages which must be withstood by the components of Figure 1B, each of the component elements illustrated in Figure 1B is preferably implemented as a discrete device. The combination of higher voltage discrete transistors (represented by the components of Figure 1B) driven by an integrated circuit providing mode switching and signal amplification, minimizes the total cost of the entire circuit. The operational amplifier and switching portions of the circuit may be implemented on an integrated circuit as will be discussed further. Meanwhile, the high-powered output portion is optimally manufactured at a discrete level. Taking this manufacturing approach, the total cost of the circuit of Figure 1A and 1B is kept to a minimum.

Another advantage of the present invention is its ability to operate off of very small current (tens of milliamps) from the power supply, even under worse case conditions. Drawing such a small amount of current from the power supply allows the present invention to utilize a capacitive input power supply. A capacitive input power supply is well known to power supply designers as a low cost supply. The prohibitive factor associated with the capacitive input type of power supply is that it is limited in the amount of current it can deliver (generally not exceeding 50 milliamps). However, it more than compensates for this fact by its ability to generate higher voltages

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which translate into high power output (recall that power is equal to the product of voltage times current). By minimizing the current drawn from its supplies, the present invention is able to benefit from the use of a capacitive input type of power supply. That is, the present invention relies upon a relatively large operating supply potential (e.g., 24 volts) compensated by a relatively low supply current (approximately 40 milliamps), to achieve maximum power output.

This result is accomplished by means of the large voltage gain provided by transistor 59 coupled with the large current gain of the output stage, and by the 3:1 turns ratio associated with transformer 90. It is appreciated that transformers not only transform impedance but they also modify voltage levels. By way of example, for transformer 90 of Figure 1B, the voltage level on the amplifier side is nominally three times larger than the voltage level present on the line side. But at the same time, the transformer provides three times the current drive capability on the line side, with the benefit of smaller supply currents on the amplifier side. The present invention employs large operating supply potentials at the output stage in combination with the 3:1 turns ration of transformer 90 to transform the high voltage associated with the amplifier side of the coil into a low voltage on the line side. (Obviously, other turns ratios may be used with similar results.)

On the other hand, current draw from the amplifier's power supply is minimized by means of the 3:1 turns ratio. That is, the current drive capability on the line side is three times greater than the current drawn from the power supply on the amplifier side of transformer 90. The low power supply currents then allow the use of the inexpensive capacitive input type of power supply.

Because an amplifier driving a power line communications system experiences widely varying receptacle impedances, assurances must be taken to prevent oscillations from occurring. This is often a difficult challenge in amplifier design. To provide stability against oscillations, the present invention incorporates lead/lag compensation networks coupled to op

amp 23. The lead compensation network circuitry comprises resistor 31 and capacitor 33 coupled in series between nodes 35 and 29. Lag compensation is provided by the feedback network comprising resistors 21, 24 and capacitor 22. At the frequency where the gain of the amplifier plus the gain or loss of the feedback network is unity, the lead and lag compensation networks guarantee at least 45° of phase margin.

Figure 2 illustrates the input impedance looking in from the power line of the circuit as a function of frequency. The operating frequencies of concern are indicated as being 118 kilohertz and 134 kilohertz for the current embodiment. The impedance is depicted by waveform 91. The lower impedance at frequencies below 118 kilohertz is primarily due to the magnetizing inductance of transformer 90. At frequencies above 134 kilohertz, the low impedance is due to the presence of parasitic capacitance. The impedance in the region of 118 KHz to 134 KHz is set primarily by resistor 81 and capacitor 82. Note that the valve of resistor 81 must be limited to avoid excessive ringing causes by noise present on the power line.

To be useful in driving power line communication systems, the amplifier circuit of the present invention also must have low harmonic distortion. Basically, FCC and Class B government regulations prohibit conducting more than 250 microvolts of noise across any portion of the broadcast band. Emissions tests are performed to meet these regulations by use of a network which results in approximately 100 ohms across the hot and neutral power lines in the pertinent frequency range. The power lines are then measured to determine how much noise is being passed onto the lines. Because of the operating frequencies involved (e.g., 118 KHz and 134 KHz), there is a potential for a fifth harmonic to fall within the A.M. broadcast band.

Low harmonic distortion is attained in the present invention by enclosing the entire amplifier circuit -- not only just the operational amplifier itself, but the operational amplifier as well as the output buffer

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circuitry -- within the feedback loop. In other words, the feedback connection back to the positive input of operational amplifier 23 is taken from the output node of the amplifier driver circuit at node 68. This feedback path from node 63 to node 28 includes resistors 66, 67, 70, 71 and capacitor 72. The fact that the feedback connection is around the whole amplifier -- including the output buffers, instead of simply operational amplifier 23 alone -- means that the present invention realizes distortion levels of better than 68dB below the fundamental when driving a 100 ohm resistive load.

Furthermore, amplitude distortion (i.e., signal clipping) is similarly avoided when driving low receptacle impedances on the order of 1 ohm. Consider the simplified alternative embodiment shown by the circuit diagram of Figure 3. Rather than employing separate resistors 70 and 71 coupled to the emitters of transistors 61 and 52, respectively, the schematic of Figure 3 shows the feedback resistors merged into a single equivalent resistance 92 connected to node 63. With this type of feedback, the open loop output impedance of the amplifier is approximately $R_B/2$. (Note that the purpose of resistors 66 and 67 is to provide a stable DC quiescent current for the two output transistors 52 and 61). With the loop closed, the output impedance looking into node 63 is approximately 0 ohms. The equivalent resistance between node 63 and 80 is shown in Figure 3 by resistor R_O.

The problem with the alternative feedback scheme of Figure 3 is that when the output stage has to drive a very small load impedance (one ohm or less) a significant amount of extra current is generated. This extra current drops additional voltage across resistors 66 and 67 which limits the voltage clipping level at node 63. In other words, the peak-to-peak voltage swing of the signal appearing at output node 63 must be reduced to avoid incurring amplitude distortion. The consequence of this extra drop means that less power is delivered onto the communication lines.

Contrast the alternative embodiment of Figure 3 with the current embodiment shown in Figure 4, once again in simplified form. Instead of

making the feedback connection directly to node 63, the embodiment shown in Figure 4 has feedback connections to nodes 64 and 65; that is, directly to the emitters of the output devices. Also, the single feedback resistor of Figure 3 is shown being split into a pair of feedback resistors 70 and 71. By splitting the feedback resistor into two separate resistors and coupling them directly to the emitters, the amplifier is able to reduce the value of the resistance of R_O by $R_B/2$ for the same output impedance seen looking in from the power line.

This result is significant since it allows the resistance value between nodes 63 and 80 to be reduced in value. So in effect, a portion of the previous resistance R_O has now been embedded into the amplifier. The net result is that an additional 2 dB of output signal range is achieved before clipping occurs. In other words, the key difference between the schematics of Figures 3 and 4 is that in Figure 4, the series output resistor between node 63 and 80 can be made smaller by $R_B/2$ to provide extra signal headroom. It is appreciated that the resistance R_O , i.e., resistors 75 and 76 as shown in Figure 1B, is required to keep the amplifier operating in a linear mode when presented with a very low impedance on the line. Linear operation guards against voltage or current clipping.

Figures 5A and 5B are a circuit schematic diagram of the current embodiment of the present invention including specific component types and values. Note that the circuit of Figures 5A and 5B includes several EXCLUSIVE-OR logic gates together with extra associated circuitry. Practitioners in the art will appreciate that the purpose and function of this circuitry is to eliminate possible glitches which might occur while switching from transmit to receive mode and vice-a-versa. Of course, certain embodiments and applications may not require such circuitry, or may employ other components for similar reasons. This additional circuitry is not deemed to be essential to the present invention.

Whereas many alternations and modifications to the present invention will no doubt become apparent to a person of ordinary skill in the art after

having read the foregoing description, it is to be understood that the particular embodiments shown and described by way of illustration are in no way intended to be considered limiting. Therefore, reference to the details of these embodiments is not intended to limit the scope of the claims which themselves recite only those features regarded as essential to the invention.

CLAIMS

I Claim:

1. An amplifier circuit for driving a power line communications system comprising:

a first circuit means for amplifying a transmit signal consistent within a first operating potential range;

a second circuit means for further amplifying said transmit signal consistent within a second operating potential range, wherein said second range is larger than said first range;

a transformer means for coupling the amplified transmit signal output by said second circuit means to said power line communications system;

feedback means coupled from the output of said second circuit means to an input of said first circuit means for maintaining a low output impedance while the amplifier circuit is in a transmit mode of operation; and

control means coupled to said second circuit means for switching the amplifier circuit from said transmit mode to a receive mode of operation,

said second circuit means presenting a relatively high impedance to the power line at the frequencies of operation while in said receive mode and a relatively low impedance while in said transmit mode.

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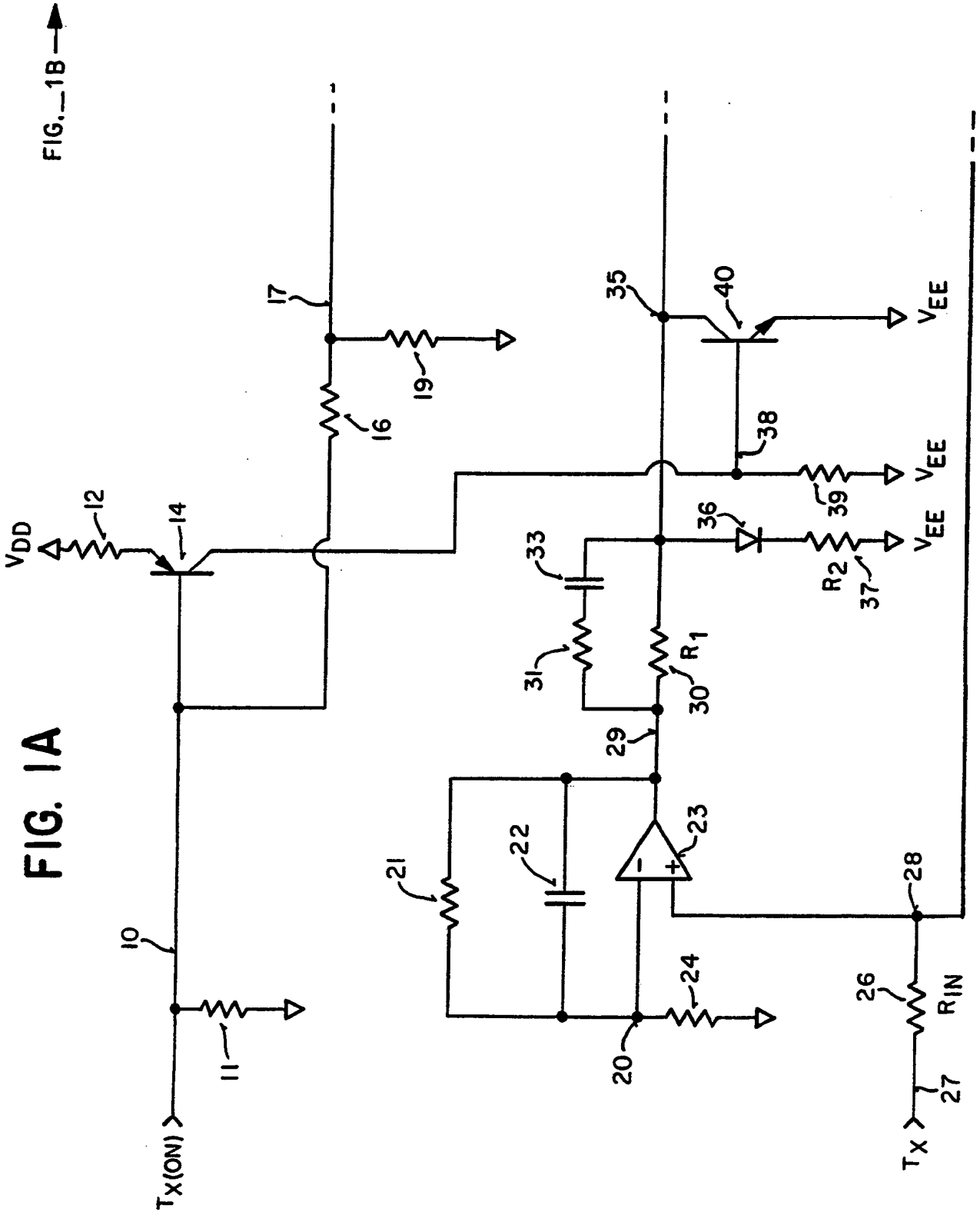

FIG. 1A

SUBSTITUTE SHEET

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FIG. 1B

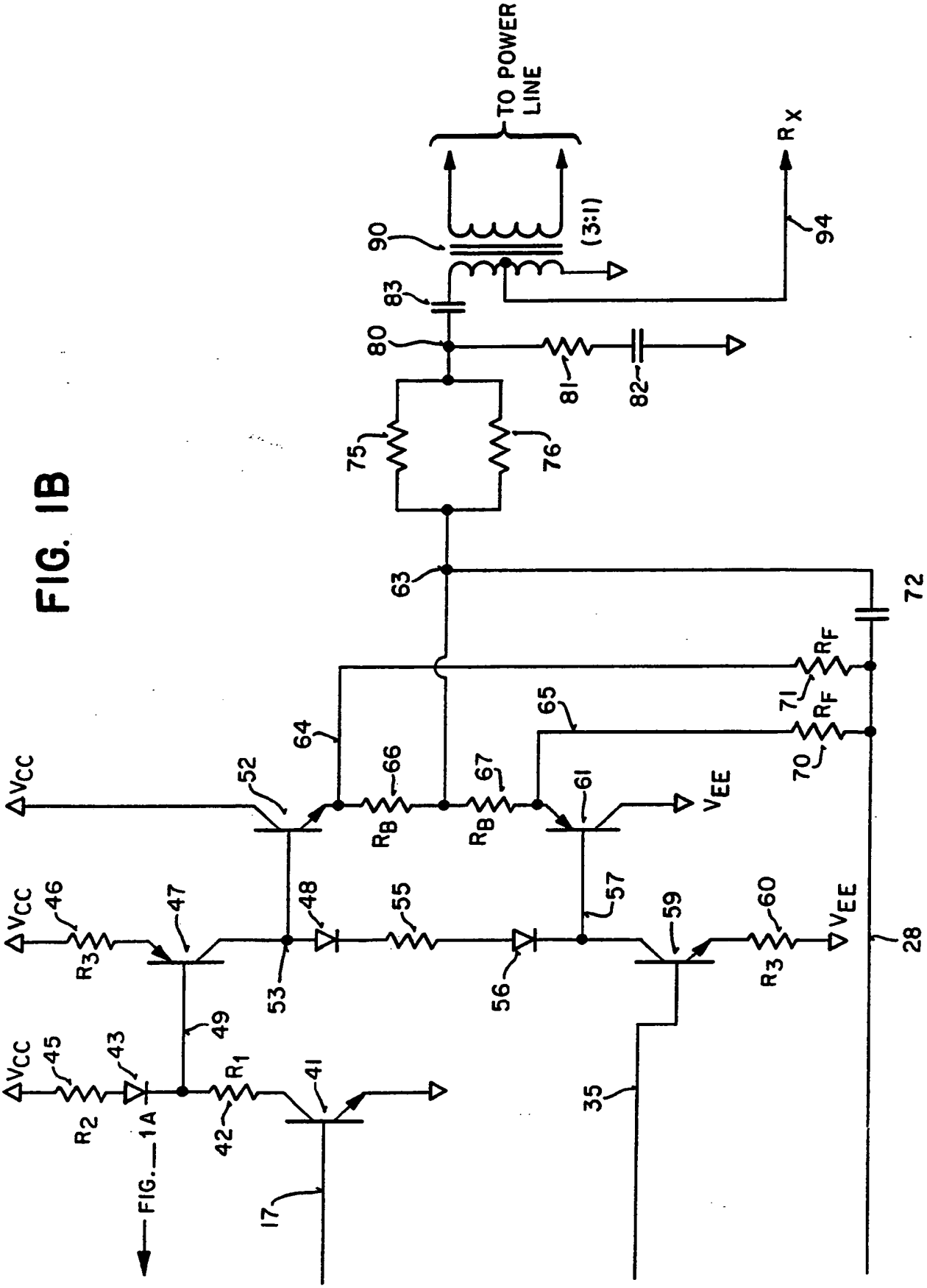

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FIG. 2

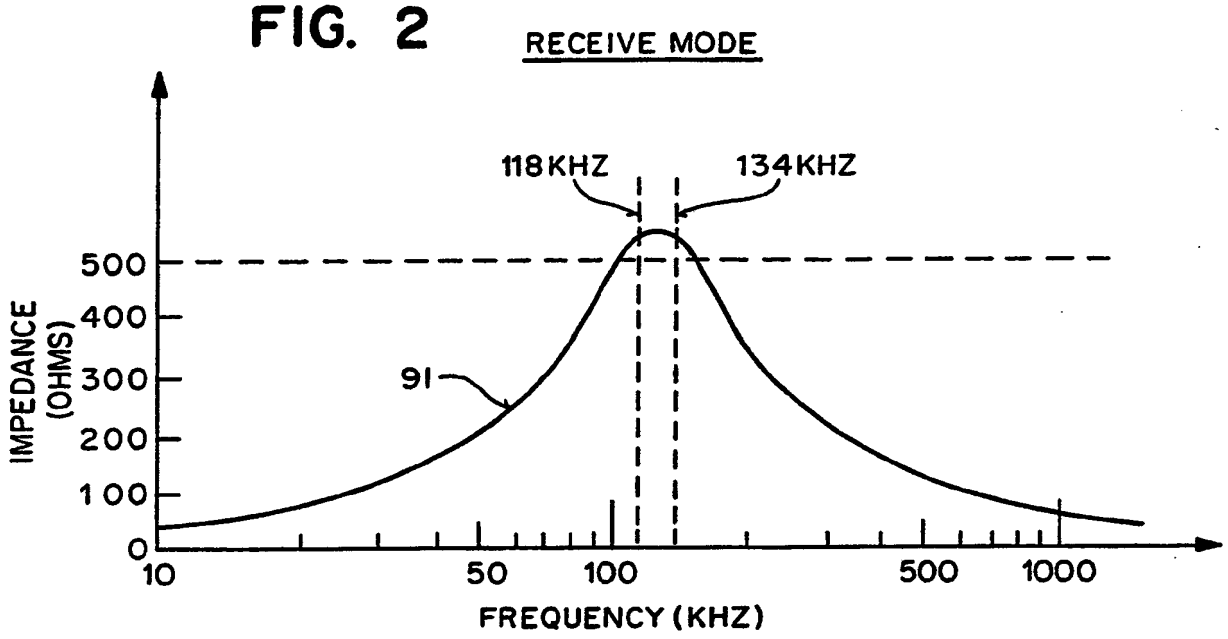
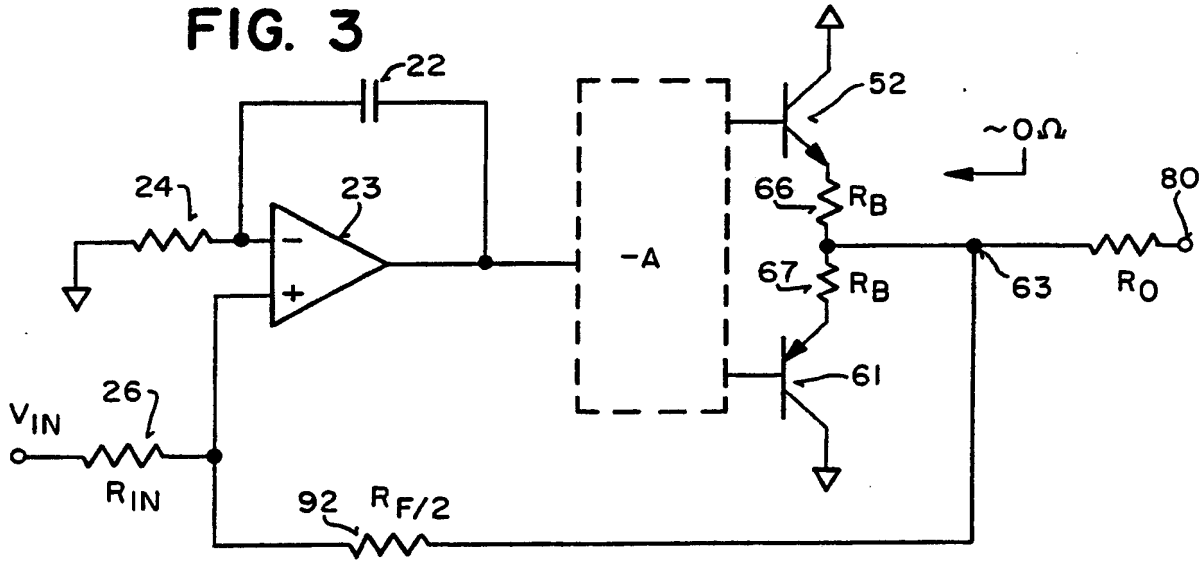


FIG. 3



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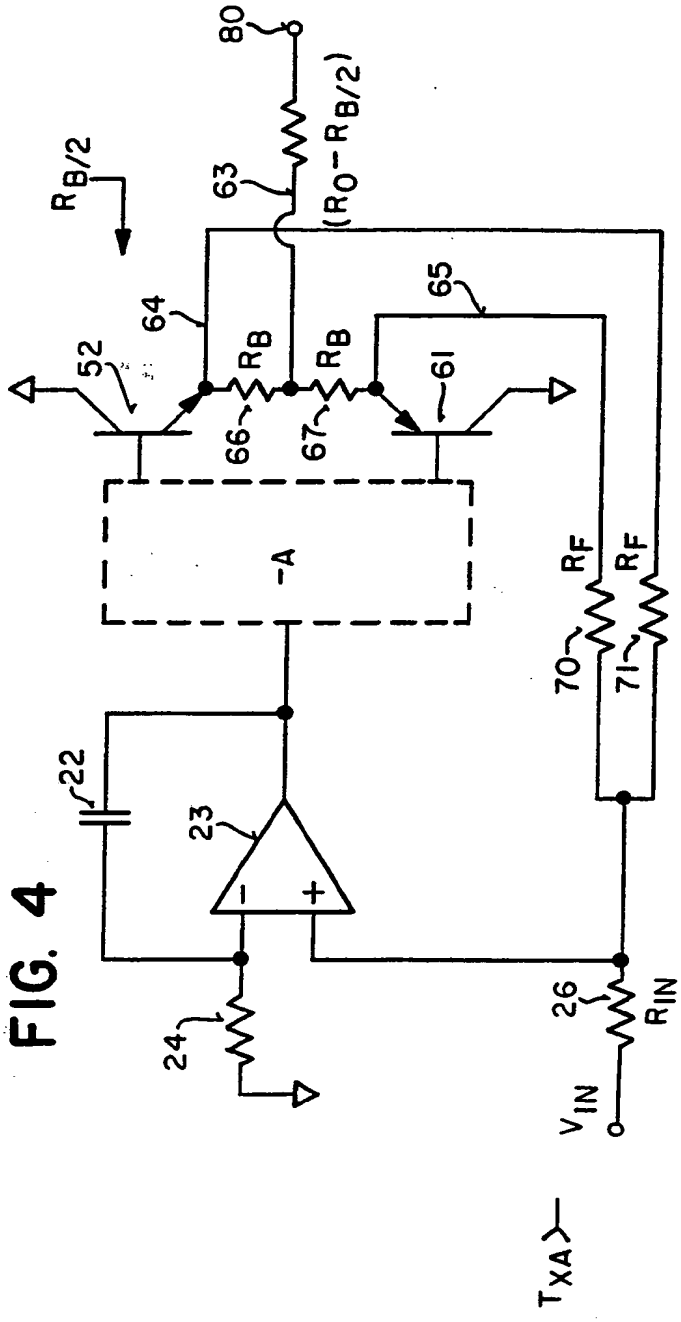

FIG. 4

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FIG. 5A

FIG. 5B →

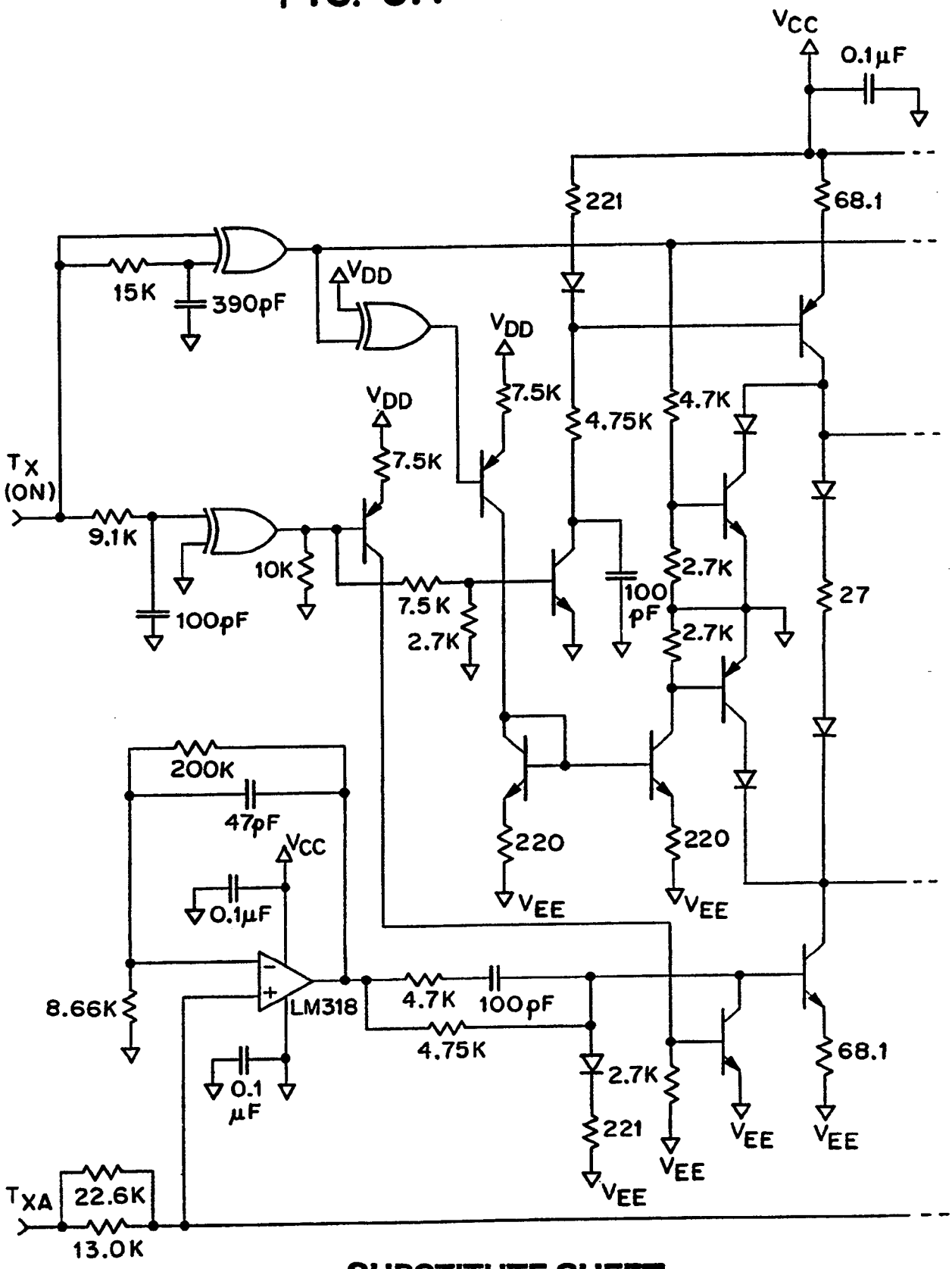

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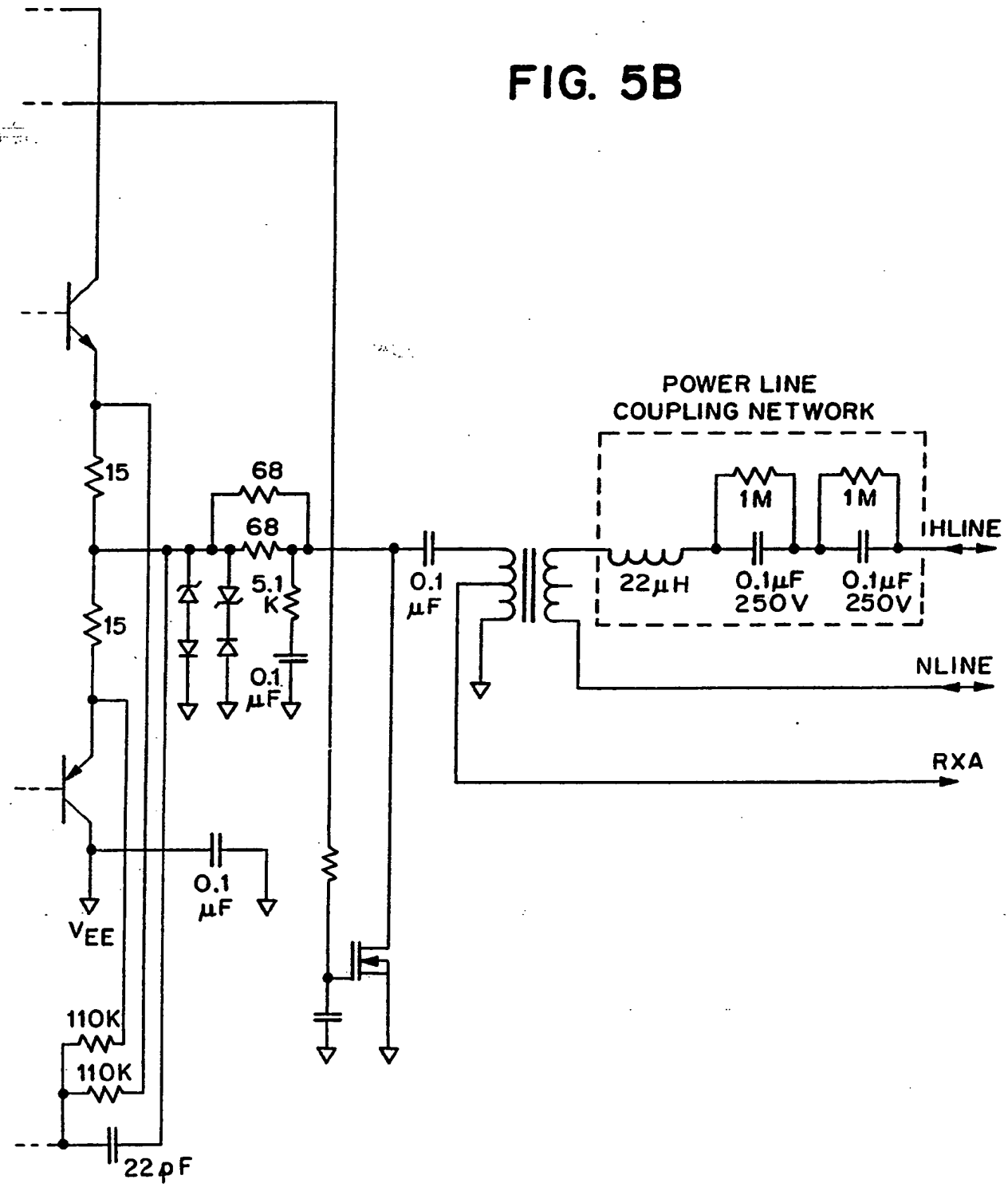
FIG. 5A

FIG. 5B



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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/03806

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H03F 1/34; H04M 11/04
US CL :330/293
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 330/51,195,196; 340/310R,310A,310CP

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 4,451,801 (MONTICELLI) 29 May 1984, See Fig. 2. and col. 4, lines 44-55.	1
X	US, A, 4,746,897 (SHUEY) 24 May 1988, See Fig. 1 and cols. 5 and 6, lines 45-68, 1-31.	1

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 12 AUGUST 1992	Date of mailing of the international search report 07 OCT 1992
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer for JAMES B. MULLINS Telephone No. (703) 308-4912

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